Transmission Lines and Passive Elements for Multilayer Coplanar Circuits on Silicon

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***Abstract*— In this paper, propagation properties of both standard and multilayer coplanar lines on different types of silicon substrates, as well as a number of quasi-lumped and stub-type circuit elements, are investigated. For the transmission lines, emphasis is placed on losses. As examples for circuit elements, a lumped parallel resonator and a high–low impedance low-pass filter are demonstrated.**

***Index Terms*— Coplanar, multilayer, passive components, silicon, transmission lines.**

I. Introduction

MONOLITHIC microwave integrated circuits (MMIC's) include a variety of transmission-line structures and quasi-lumped components like series and shunt capacitors or inductors realized in the microstrip or coplanar technique.

As a material with mature technology, silicon is increasingly used for higher frequencies as well, both on standard silicon (5–20 $\Omega\cdot$cm) as well as on high-resistivity silicon ($\geq$1000 $\Omega\cdot$cm) [1], [2], [17].

A coplanar MMIC design has well-known advantages (e.g., no via holes, no backside processing). With additional layers of dielectrics and metallization on top of a substrate, a number of modified coplanar or quasi-coplanar structures can be realized, as shown in Fig. 1.

In the top-left structure in Fig. 1, the additional dielectric layer is used to separate the coplanar line from a possibly lossy substrate. The mid-left structure represents a coplanar line with the center conductor on top of the dielectric layer, allowing the realization of higher transmission-line impedances. Overlapping of the center conductor, as shown in the bottom-left structure, yields low transmission-line impedances.

Thin-film microstrip structures can also be realized with this technique, as shown by the bottom-right structure in Fig. 1, and can be easily connected to the coplanar line with elevated center conductor.

Stronger broadside coupling of coplanar lines is easily achieved using the mid-right structure. With the use of another dielectric and metallization layer, broadside coupling can also be obtained for the thin-film microstrip lines (upper right structure in Fig. 1), e.g., allowing the realization of couplers [3].

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Materials typically used for dielectric layers and passivation in MMIC's include silicon oxides and nitrides, as well as organic compounds like polyimide and benzocylobutene (BCB) [4]. The dielectric layer thickness typically ranges from 0.2 μm (Si_3N_4 passivation) to several micrometers (SiO_2, polyimide), as does the metallization thickness.

Very complicated three-dimensional multilayer structures have been shown using several polyimide and metallization layers [5].

II. Modeling of Multilayer Coplanar Structures

An improved modeling of the propagation constant and loss of transmission lines, as well as of the scattering parameters of discontinuities, has to account for substrate material losses, passivation layers, finite metallization thickness, and conductor loss.

Due to the finite conductivity of the metal, the field penetrates into the conductors, with the skin depth being

$$a = \frac{1}{\sqrt{\pi f \mu_0 \sigma}}.$$

For gold with a conductivity of $\sigma = 4.2\cdot 10^7$ $[\Omega\cdot\mathrm{m}]^{-1}$, the skin depth is about 0.8 μm at a frequency of 10 GHz, which is in the same order of magnitude as the metal and dielectric thickness considered here. This has a considerable influence especially on thin-film microstrip and parallel-plate-like structures.

A. Parallel-Plate Waveguide Approximation

For thin-film structures (as shown on the right side of Fig. 1) with strip widths much larger than the dielectric thickness h, a parallel-plate waveguide model can be used to approximately calculate propagation and attenuation constants. In this model, the structure is assumed to be infinite in the dimension perpendicular to the direction of propagation; the electric and magnetic fields are, therefore, independent of the lateral coordinate. The metallization is also assumed to be of infinite thickness.

However, due to the finite conductivity, the electric field will have a nonzero longitudinal component, and the propagating mode will be of a TM type.

By setting up the respective field equations in the dielectric and the metallization, and matching the tangential fields at the interface between metal and dielectric, an analytical equation for the propagation constant γ is obtained as follows:

$$\frac{k_y^D}{k_y^M}\cdot\frac{\sigma}{\omega\varepsilon_0\varepsilon_r}\cdot\frac{\sin(k_y^D h/2)}{\cos(k_y^D h/2)}+1=0.$$

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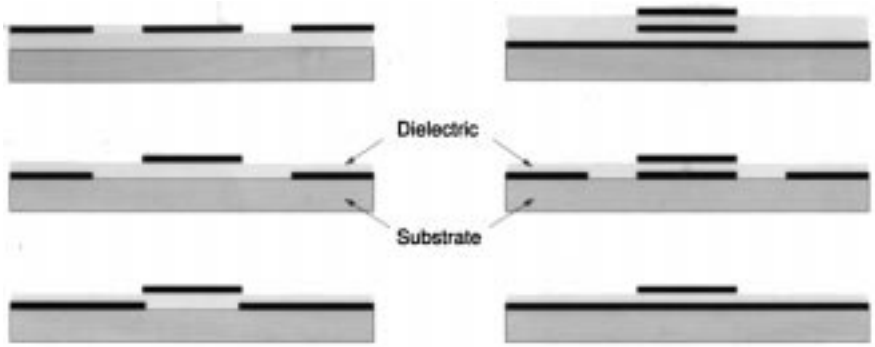

Fig. 1. Some examples of multilayer structures using additional dielectric and metallization layers on top of a silicon substrate.

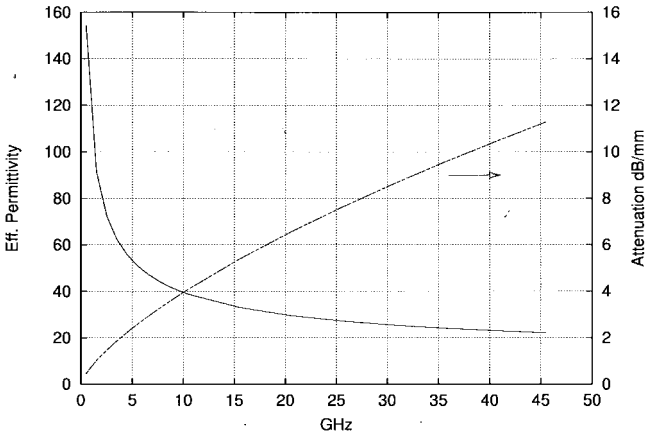

Fig. 2. Effective permittivity and loss of a thin-film microstrip line with 200-nm Si_3N_4 dielectric, calculated with the parallel-plate waveguide approximation.

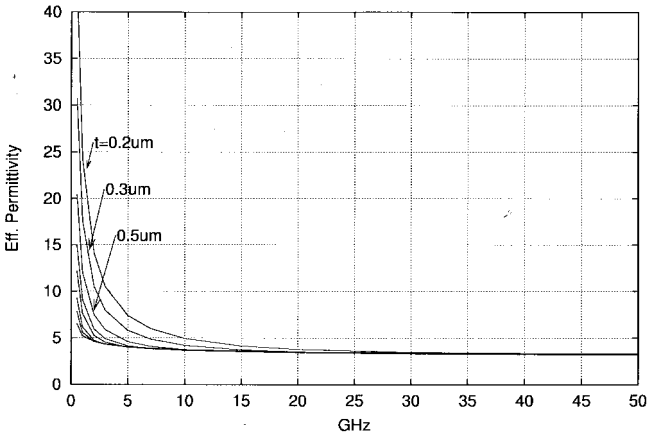

Fig. 3. Effective permittivity of a thin-film microstrip line on 2-μm polyimide versus conductor thickness t.

The wavenumbers perpendicular to the metallization plane in the dielectric (D) and metal (M) region are given by

$$k_y^D = \sqrt{\gamma^2 + \left(\frac{\omega}{c_0}\right)^2 \varepsilon_r} \quad k_y^M = \sqrt{\gamma^2 - j\omega\mu_0\sigma}.$$

The solution of this equation can be done in an extremely short time compared to full-wave methods, thus it can easily be included into standard computer-aided design (CAD) and optimization procedures. The computation of a thin-film microstrip line with a 200-nm Si_3N_4 dielectric using this model shows a very steep increase of the effective permittivity toward lower frequencies (see Fig. 2) for a nominal permittivity of 7.45 and gold metallization. The high attenuation in the gigahertz-frequency range limits the use of this type of thin-film structures.

B. Mode-Matching Technique

For general transmission-line structures with finite metallization thickness, a full-wave analysis has to be performed [6]–[9].

Finite conductivity can be taken into account by introducing the complex permittivity

$$\varepsilon = \varepsilon' + \frac{\sigma}{j\omega}$$

with the conductivity σ in the imaginary part. The fields are then computed inside metal structures in the same way as for dielectric areas.

In this paper, the computation of transmission-line parameters is performed with a mode-matching software provided by Schmidt [9]. Results of the computation for some of the structures in Fig. 1 will be shown below.

When the dielectric height of the thin-film microstrip line is in the same order of magnitude as the skin depth, the effective permittivity and loss depend strongly on the conductor thickness, as can be seen in Figs. 3 and 4, for a 10-μm-wide line of gold metallization on top of a 2-μm polyimide layer with a nominal permittivity of 3.5. The characteristic impedance of this microstrip line is about 30 Ω.

Increasing the dielectric thickness yields lower loss and less dispersion at low frequencies.

The realizable transmission-line impedance using a coplanar line with center conductor on top of a 5-μm polyimide layer (mid-left structure in Fig. 1) is shown in Fig. 5 for varying linewidth and constant ground-to-ground spacing of 200 μm. Due to the lower effective permittivity, higher transmission-line impedances can be achieved with the same linewidth compared to standard coplanar lines placed directly on the substrate [10]. Center conductor widths larger than 200 μm are overlapping the ground plane and, therefore, approach the structure of thin-film microstrip lines.

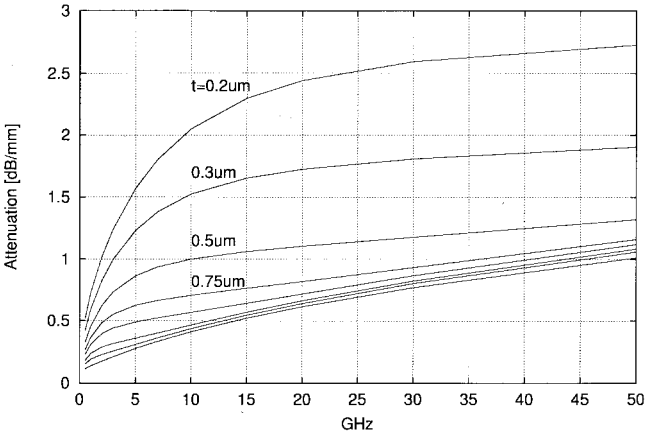

Fig. 4. Attenuation of a thin-film microstrip line on 2-μm polyimide versus conductor thickness t.

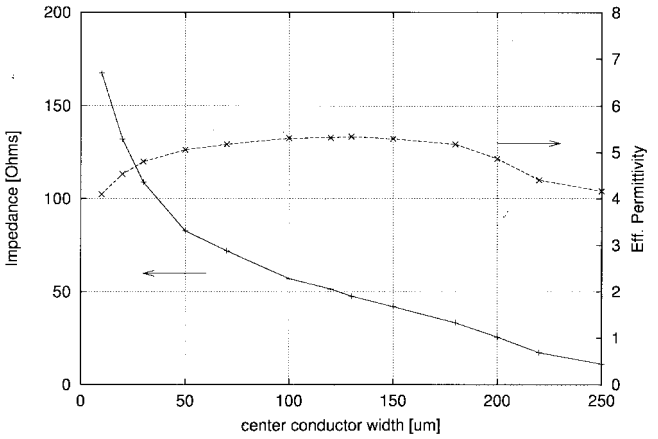

Fig. 5. Transmission-line impedance and effective permittivity of a coplanar line with elevated center conductor on 5-μm polyimide and 200-μm ground spacing as a function of linewidth.

Broadside coupled coplanar lines, as shown in the mid-right example of Fig. 1, seem to be well suited for the realization of couplers. With the dielectrics used here, there is a large difference in the effective permittivity of the two modes that propagate in this structure. The even mode, which is similar to a coplanar mode, has a permittivity of approximately 7.0 at higher frequencies (for 50-μm ground spacing), while the odd mode, which is similar to a parallel-plate mode, has a permittivity of 3.2. Quarter-wavelength-type couplers using this structure will, therefore, not work well. However, with another dielectric and metallization layer, quasi-ideal couplers become realizable [11].

III. Theoretical Results and Measurements of Transmission-Line Properties

The influence of conductor and substrate loss on the propagation along the coplanar waveguide will be presented in this section. Different coplanar-line geometries are investigated, with 20-μm linewidth and 15-μm gap width resulting in 50-μm ground-to-ground spacing, with 50-μm linewidth and 25-μm gap width (100-μm ground-to-ground spacing),

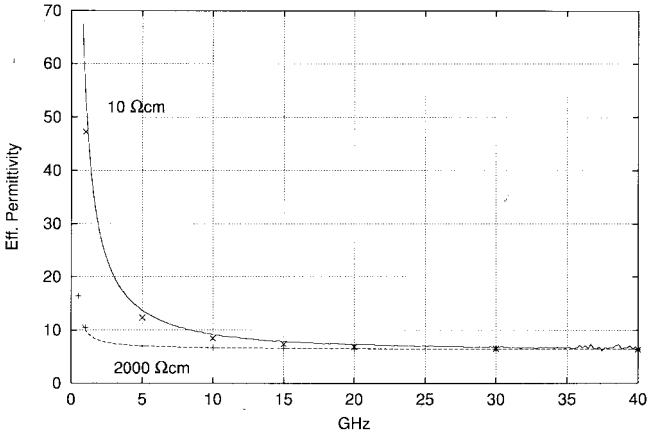

Fig. 6. Effective permittivity of coplanar lines with 50-μm ground spacing on 2000-$\Omega \cdot$ cm silicon (bottom trace) and on 5–20-$\Omega \cdot$ cm silicon (top trace). Solid lines represent measured values, the symbols $+$ and $\times$ represent computed values.

and with 100-μm linewidth and 50-μm gap width (200-μm ground-to-ground spacing). All three configurations exhibit a characteristic transmission-line impedance of about 50 Ω.

The metallization in all the following examples is made of evaporated titanium and gold, with a thickness of 50 and 300 nm, respectively, patterned by liftoff. The multilayer structures were realized using a photosensitive polyimide $(\varepsilon_r = 3.5)$, which can be spun on and patterned like a conventional resist.

The measurements were performed on-wafer using a thru-reflection line (TRL) calibration technique. Line lengths for the "delays" were 9.5 and 1.2 mm (between the reference planes) for structures placed directly on silicon, and 11.8 and 1.35 mm for those placed on top of the polyimide layer. A short circuit was used as "reflect."

A. Effective Permittivity

Due to the skin effect, the effective dielectric constant of standard coplanar lines increases at low frequencies [6], [7]. This can be clearly seen both in theory and experiment in the lower trace in Fig. 6 for 2000-$\Omega \cdot$ cm silicon. For standard silicon, an additional large increase of the permittivity exists at low frequencies (slow-wave effect) due to the substrate loss.

Besides this, the most interesting parameter of coplanar transmission lines on silicon is loss. Measurements [12], [13] have shown that high-resistivity silicon is nearly as good a substrate for microwave and millimeter-wave MMIC's as GaAs and InP [14].

B. High-Resistivity Silicon

The largest contribution to the losses at higher frequencies is the finite conductivity of the metallization. Losses due to a 2000-$\Omega \cdot$ cm silicon substrate can nearly be neglected.

Fig. 7 shows losses for standard coplanar lines with different ground-to-ground spacing on 2000-$\Omega \cdot$ cm silicon. The solid lines represent measured values, while the symbols show computed losses for the real lossy substrates and for an ideal lossless substrate. As can be clearly seen, the substrate losses

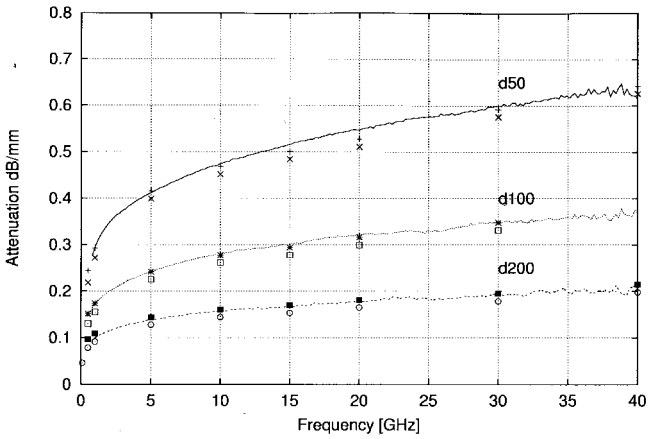

Fig. 7. Losses of coplanar lines on silicon (2000 Ωcm), with 50-μm ground spacing denoted by $d50$, with 100-μm ground spacing denoted by $d100$, and with 200-μm ground spacing denoted by $d200$. Solid lines represent measured values, the symbols $+$ $*$ ■ represent computed values for the real substrate, and $\times$ □ ∘ represent computed values for an ideal substrate.

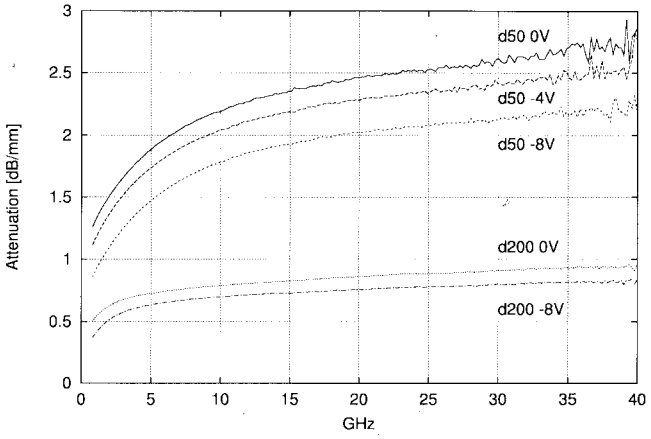

Fig. 8. Losses of coplanar lines on top of silicon (2000 Ωcm) with a 200-nm Si_3N_4 passivation layer, also with bias voltage applied between center conductor and ground plane (-4 V, -8 V).

represent only a minor contribution to the overall losses. The ohmic losses increase with smaller gap widths.

GaAs MMIC's typically have a silicon–nitride passivation covering most of the chip area. However, for coplanar transmission-line structures on silicon, this leads to high losses due to charge buildup at the interface Si–Si_3N_4, similar to the Si–SiO_2 interface [15]. Loss measurements of coplanar lines on top of 2000-$\Omega \cdot$cm silicon covered with 200-nm Si_3N_4 are shown in Fig. 8.

The presence of charged states can be demonstrated by applying a bias between the center conductor and the ground plane of the coplanar line. Negative bias reduces the loss significantly, especially for the smaller line geometry (Fig. 8). Applying a positive bias voltage, losses are increased only slightly.

This effect is avoided by removing the passivation in the gaps of the coplanar line after the patterning of the metallization [16].

C. Doped Layers on High-Resistivity Silicon

Active devices in microwave and millimeter-wave MMIC's generally are fabricated using different doped layers on top of semi-insulating GaAs or high-resistivity silicon. The doped layers usually are made by implantation or epitaxial growth, either selectively or on the whole surface of the wafer. The realization of integrated circuits with active devices, transmission lines, and passive structures can get difficult if losses due to the conductive substrate layers become too high. The doped layers investigated here are similar to those used for silicon Schottky diodes described in [17, p. 250].

In a first step, a 6000-$\Omega \cdot$cm silicon sample with a 3-μm implanted n^+ layer (with $5 \times 10^{19}/\text{cm}^3$ doping concentration at the surface) is used. Coplanar lines placed on this sample show no propagation, the conductive layer acts like a short circuit.

Next, a transmission line on an epitaxially grown n^- layer ($3 \times 10^{16}/\text{cm}^3$) of 600-nm thickness, again on 6000-$\Omega \cdot$cm silicon, is measured, as shown in Fig. 9. The coplanar lines on this substrate have an attenuation about twice of those on 2000-$\Omega \cdot$cm silicon, as shown in Fig. 8, but are still usable if the lines are not too long. Thus, removing the doped layer underneath the coplanar lines is not always necessary.

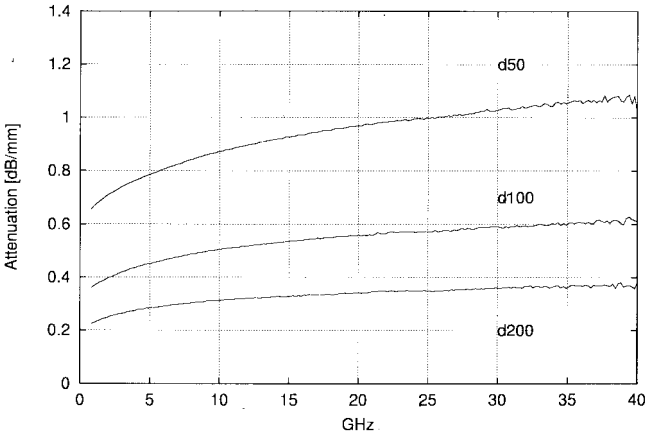

Fig. 9. Losses of coplanar lines on top of a 600-nm n^- epitaxial layer on high-resistivity silicon (6000 $\Omega \cdot$ cm).

D. Standard Silicon

Standard silicon with a resistivity of 5–20 $\Omega \cdot$cm is used in conventional silicon processes. It is also interesting for silicon MMIC's at higher frequencies because of lower cost. In addition, various processing steps can significantly reduce the resistivity of high-resistivity silicon, resulting in similar properties as with standard silicon.

Coplanar lines placed directly on top of standard silicon show high attenuation, as shown in Fig. 10. To avoid this problem, modifications of the transmission-line structure are investigated.

Isolating the coplanar line from the conductive silicon using a 0.2-μm silicon–nitride layer does not improve the situation; the loss increases again due to the presence of charged states. However, with a thick layer of polyimide, losses can

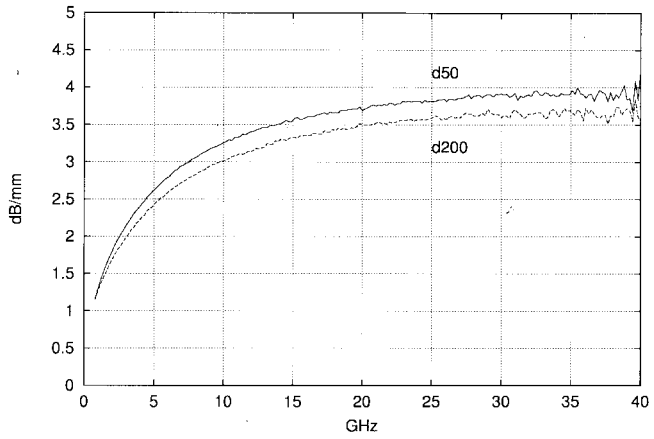

Fig. 10. Loss of coplanar lines on standard silicon 5–20 $\Omega \cdot$ cm.

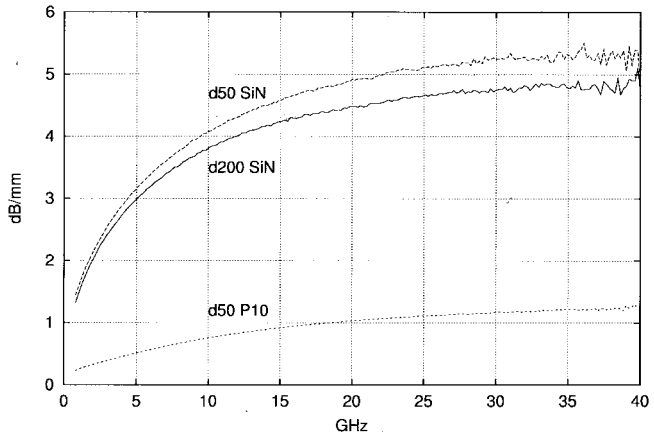

Fig. 11. Loss of coplanar lines on top of a dielectric on standard silicon (5–20 Ωcm), $d50$ SiN and $d200$ SiN denote a 200-nm Si_3N_4 dielectric and 50-μm or 200-μm ground spacing, respectively. $d50\ P10$ denotes a 10-μm polyimide dielectric and 50-μm ground spacing.

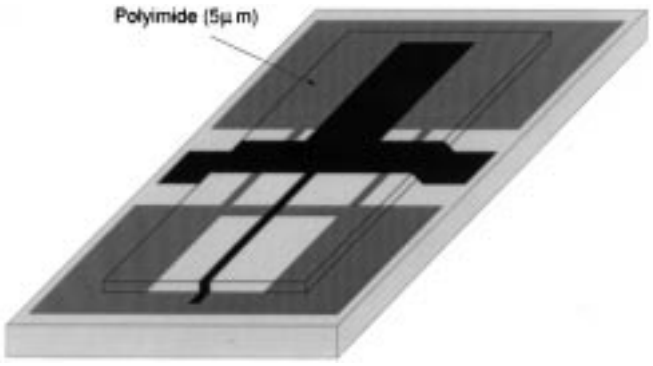

Fig. 12. Parallel *LC* resonator using a low-impedance thin-film microstrip open stub (upwards) and a high-impedance elevated coplanar shorted stub (downwards).

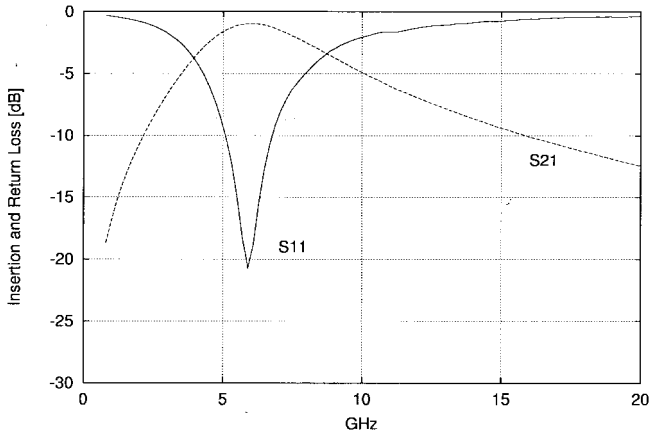

Fig. 13. Measured S-parameters of the *LC* resonator with plated metallization.

be reduced to an acceptable level, especially when the gap width of the coplanar line is in the order of the thickness of the dielectric layer, as shown in Fig. 11 for 50-μm ground spacing and 10-μm polyimide thickness. The width of the center conductor of this line is set to 34 μm to maintain a characteristic impedance of 50 Ω.

IV. Quasi-Lumped-Element Structures on High-Resistivity Silicon

Coplanar lines with elevated center conductor can be used for high-impedance transmission lines while keeping a reasonable linewidth, as shown in Fig. 5. Together with thin-film microstrip structures, which easily allow the realization of very low transmission-line impedances, a number of quasi-lumped element structures can be built. The examples shown here are realized on 2000-$\Omega \cdot$ cm silicon substrate, with a 5-μm polyimide dielectric layer and evaporated or plated gold metallization.

Fig. 12 shows a parallel *LC* resonator with a quasi-lumped capacitor realized using a thin-film microstrip open stub and a quasi-lumped inductor made of a shorted segment of coplanar line with elevated center conductor. The dielectric used here is 5-μm polyimide, and the ground-to-ground spacing of the coplanar line is 200 μm. Characteristic impedances are about 4.0 and 140 Ω for the microstrip and elevated coplanar lines, respectively, while the line length is 700 μm for both stubs. Overall length of the resonator is, therefore, about 1.5 mm for a resonant frequency of 6 GHz, compared to a quarter-wavelength of about 5 mm for a coplanar line at this frequency.

To prevent the propagation of unwanted modes, conductive bridges can easily be placed around the tee junction between silicon and polyimide using this multilayer technique. The gold thickness on this sample is increased to 2.5 μm by plating to reduce conductor losses.

The passband loss of this resonator is about 1 dB, as shown in Fig. 13, while the bandwith is quite large because of the low-Q factor due to the direct coupling to the 50-Ω connecting lines. A less tight coupling (e.g., using series capacitors) will result in smaller bandwidth, but at the expense of higher passband loss. Together with series *LC* resonators, bandpass filters of moderate bandwidth can be designed.

Fig. 14 shows a stepped impedance low-pass filter [18] realized with thin-film microstrip line segments of low transmission-line impedance, and high-impedance coplanar

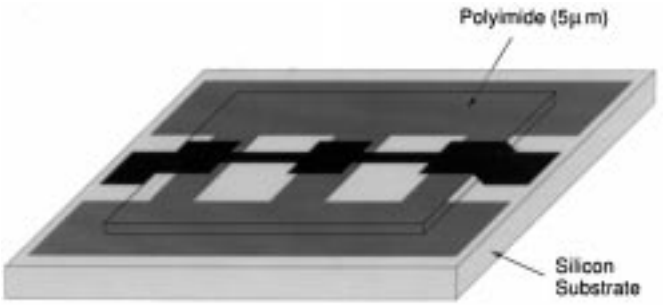

Fig. 14. Stepped impedance low-pass filter, alternating low-impedance thin-film microstrip and high-impedance elevated coplanar line segments.

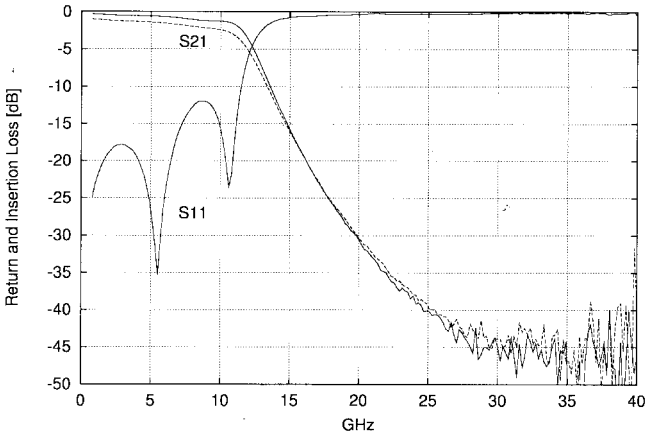

Fig. 15. Measured S-parameters of the stepped impedance low-pass filter, with plated metallization ($S11$ and upper $S21$ trace) and thin metallization (lower $S21$ trace).

line segments with elevated center conductor on 5-μm polyimide. Characteristic impedances are about 2.5 and 140 Ω for the microstrip and elevated coplanar lines, respectively, while the line length are 118 μm for the first and last microstrip segment, 174 μm for the center microstrip segment, and 1245 μm for both coplanar segments.

Acceptable losses of less than 1.3 dB in the passband can be achieved (Fig. 15), using a plated metallization of 2.5-μm thickness, while an evaporated metallization of 0.3 μm shows a loss of about 2.5 dB, which is comparable to a previously realized structure on GaAs with 2-μm polyimide and 1-μm metallization thickness [18]. For the given 10–12-GHz corner frequency, the low-pass filter requires a chip area of 1.5 mm^2 only.

V. Conclusion

Transmission-line loss investigations of coplanar waveguides on silicon show that high-resistivity material is required for low attenuation, which then is comparable to the attenuation of coplanar lines on GaAs or InP. Microwave and millimeter-wave MMIC's can, therefore, equally be realized on silicon. Additional dielectric layers on top of the substrate allow the use of standard or doped silicon, and allow the realization of combined coplanar and thin-film microstrip structures.

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Dr. Schumacher was the recipient of the University of Ulm's Academic-Industrial Cooperation Award in 1995.